



Intel® 41110 Serial to Parallel PCI Bridge BSDL Hardware Test Validation

White Paper

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Shortened Product Name

Revision History

Date	Revision	Description
August 2006	001	Initial release



1.0 BSDL Hardware Validation

The test validation test was performed on the BSDLWorks™ Test Fixture.

Test software was a ScanWorks 3.7 project utilizing three test actions. The i41110_R1 device **passed** all tests run as described in section 2.1.3

1.1 BSDL Syntax & Semantics

The following BSDL file was used:

- i41110_R1
where _R1 indicates first validated release

1.2 BSDL Hardware Test Validation Detail

This section provides detail on the results of the ScanWorks 3.7 boundary scan validation of BG567 package type. One (1) device was used in the validation.

1.2.1 Materials Used

The following materials were used during validation:

- Test adaptor ADA1163
- BSDL files: I41110_R1
- ScanWorks INTEL 41110 Project
- 1 device with no markings.

1.2.2 Tests Performed

The following tests were performed on 1 device:

1. Data Register Test
Scan Path ATPG uses only DR scans on the bypass registers or, if present, the IDCODE registers of the boundary-scan devices. No IR scans are used in this test to prevent possible damage to the design from passing harmful values. The design being tested is left in the functional mode. For devices with secondary scan paths, only the default scan path is validated.
2. Instruction Register Test
IR Verify performs an IR Scan on the target design and checks the outputs of the instruction registers of each device from TDO to TDI. If 01 is the first two bits received from each device instruction register, the design being tested passes the test. Each IR Scan ends in Test- Logic-Reset state to minimize the possibility of damage to hardware.
3. Scan Path Verify Test:
 - Chain - checks the TDI, TDO, TMS, and TCK signals in your boundary-scan chain. If this test fails, no other tests are run.
 - Chain Length - checks the length of the boundary-scan register for each device in the boundary-scan path.
 - ID Code - tests all components that have an ID code register. This verifies that the devices with ID codes match those defined in your BSDL description, in the order described in the scan path.



- Usercode – tests all components that have a usercode register. This verifies that the devices with usercodes match those defined in your BSDL description.
 - IR Capture - checks the instruction register capture value for all components in the selected chain. This verifies that the instruction register for each device is functioning correctly.
4. SAMPLE /EXTEST Wagner patterns
Verify proper I/O cell mapping to package pins. 100% pin-level fault coverage for stuck-at conditions, shorts, and opens on all boundary-scan cells.
 5. SAMPLE /EXTEST Walking 1 patterns
Verify output enable cell mapping to proper output cells

1.2.3 Tests Conditions

VDD_CORE : 1.50V +/- 2%
VDD : 3.30V +/- 5%

1.2.3.1 Test Results

Summary:

1 device passed all tests.

Results by Test Type (1 chip tested per type):

Power-up ID/Byp Test	0.5Mhz Clock(Mode Free Run)	Passed
Instruction Capture Test	0.5Mhz Clock(Mode Free Run)	Passed
Bypass Test	0.5Mhz Clock(Mode Free Run)	Passed
Commanded ID Test	0.5Mhz Clock(Mode Free Run)	Passed
BSR Length Test	0.5Mhz Clock(Mode Free Run)	Passed
TRST Test	0.5Mhz Clock(Mode Free Run)	Passed
Wagner Test	0.5Mhz Clock(Mode Free Run)	Passed
Walking '1&0' Test	0.5Mhz Clock(Mode Free Run)	Passed

1.3 Findings

Although most devices will operate at 4Mhz in the validation fixturing, this device could not pass testing unless run at 0.5Mhz. Possible ground bounce due to larger current draw on the 1.5v power.

1.3.1 Non-Standard Efforts

Package lid was modified to allow usage with a BGA socket.

1.4 Summary and Recommendations

Except for lower operating frequency the device is compliant with JTAG1149.1